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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,544	12/05/2003	Nicholas R. Watts	P17173	1914

7590 11/14/2005

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EXAMINER
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ANDUJAR, LEONARDO

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	<b>Application No.</b> 10/729,544	<b>Applicant(s)</b> WATTS ET AL.	
	<b>Examiner</b> Leonardo Andújar	<b>Art Unit</b> 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12 August 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 9-15, 17-19, 21, 22, 29-34 and 39 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 9-15, 17-19, 21, 22, 29-34 and 39 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date: _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date: _____  | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Acknowledgement***

1. The amendment filed on 8/18/2005 in response to the Office action mailed on 6/30/2005 has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 9-15, 17-19, 21, 22, 29-34, 36-37 and 39.

### ***Election/Restrictions***

2. Applicant's election without traverse of group I in the reply filed on 04/29/2005 is acknowledged.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 9-14 and 29-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Rokugawa et al. (US 6,44,314).

5. Regarding claims 9 and 29, Rokugawa (e.g. fig. 2 and 13) shows a substrate 14 (a first layer 14) and a coverlay (a second insulating layer laminated to the substrate and having at least one opening 30 formed in the coverlay by photolithography. Also, the coverlay is in contact with the substrate (col. 7/lls. 9-24 and figs. 6 and 17). Note that the structure of figure 13 is made by a superposing multiple layers 14 made by the process shown in figure 2 (col. 7/lls. 59-65).

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6. Regarding claim 10, Rokugawa shows that the coverlay is a flexible material such as polyimide (col. 7/lls. 9-24).
7. Regarding claims 11 and 30, Rokugawa shows that the substrate is a flexible material such as polyimide (col. 7/lls. 9-24).
8. Regarding claims 12 and 31, Rokugawa shows that the coverlay is a flexible material such as polyimide (col. 7/lls. 9-24).
9. Regarding claims 13 and 32, Rokugawa shows that the substrate has metal traces (12, 42, 46; col. 7/lls. 40-58) on a first surface of the substrate and metal ground plane (12, 42, 46) on a second surface of the substrate that is opposite to the first surface and the coverlay is laminated to the first surface of the substrate.
10. Regarding claims 14 and 33, Rokugawa shows that the metal traces and the metal ground plane are made of copper (col. 7/lls. 40-58).

***Claim Rejections - 35 USC § 103***

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 15, 17, 18, 34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rokugawa et al. (US 6,44,314) in view of Fox et al. (US 5,128,831).
13. Regarding claims 15 and 34, Rokugawa (e.g. fig. 2, 13 and 16) shows an integrated circuit (IC) package having a substrate 14 (lower layer 14); and IC 16 mounted on a surface of the substrate and a coverlay (top layer 14/41) laminated to the

substrate and having at least one opening (the opening formed in the frame 41) formed in the coverlay by photolithography (col. 7/lls. 9-24 and col. 14/lls. 1-15); and at least one conductive connection 20a formed through one of the overlays and connecting the IC. Note that the structure of figure 13 is made by a superposing multiple layers 14 made by the process shown in figure 2 (col. 7/lls. 59-65). Also, the IC is positioned in an opening of the overlay (the opening formed by the frame 41), the opening are formed by photolithography. Rokugawa does not teach that the structure may be stacked to include at least two packages. Therefore, Rokugawa does not show that the connections 20a are connected to another IC. Nevertheless, Fox (e.g. figs. 2 and 3) teaches an IC package including two or more integrated circuit packages in stacked relation to each other wherein each of the packages includes a substrate 11 and an IC 15 mounted on the substrate having conductive connections for connecting one of the ICs to another of the ICs. According to Fox, this type of embodiment is a reliable structure capable of increasing the package mounting density (col. 2/lls. 54-58 & col. 3/lls. 56-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to stack at least two of the IC packages disclosed by Rokugawa and to connect the ICs in accordance with Fox's invention in order to increase the package mounting density.

14. Regarding claim 17, Rokugawa shows that the coverlay is a flexible material such as polyimide and copper (col. 7/lls. 9-24 & col. 14/lls. 47-54).

15. Regarding claims 18 and 36, Rokugawa shows that the substrate is a flexible material such as polyimide (col. 7/lls. 9-24).

16. Claims 19-22 and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rokugawa et al. (US 6,44,314) in view of Fox et al. (US 5,128,831) in view of Blumenau et al. (US 6,421,711).

17. Regarding claims 19 and 37, Rokugawa (e.g. fig. 2 and 13) shows an integrated circuit (IC) package having a first substrate 14 (lower layer 14); and a first IC 16 mounted on a surface of the first substrate and a first coverlay (top layer 14/41) laminated to the surface of the first substrate and having at least one opening (the opening formed in frame 41) formed in the coverlay by photolithography (col. 7/lls. 9-24 and col. 14/lls. 1-15); and at least one conductive connection 20a passing through at least one of the openings in the first overlays. Note that the structure of figure 13 is made by a superposing multiple layers 14 made by the process shown in figure 2 (col. 7/lls. 59-65). Furthermore, the first IC is positioned in the opening formed by photolithography in the first coverlay. Rokugawa does not teach that the structure may be stacked to include at least two packages and a communication device couple to the first IC. Therefore, Rokugawa does not show that the connections 18 are connected to other IC and/or a second substrate positioned in stacked fashion on the first coverlay; a second IC mounted on a surface of the second substrate; a second coverlay laminated on the surface of the second substrate and having at least one opening formed by photolithography. Nevertheless, Fox (e.g. figs. 2 and 3) teaches an IC package including two or more integrated circuit packages in stacked relation to each other including a first substrate 11 and a first IC 15 mounted on the first substrate; a second substrate 11 and a second IC 15 mounted on the second substrate, having conductive

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connections for connecting the first and second ICs. According to Fox, this type of embodiment is a reliable structure capable of increasing the package mounting density (col. 2/lls. 54-58 & col. 3/lls. 56-60). Blumenau discloses a communication device such wireless data transceiver is couple to a chip to permit remote interrogation (col. 37/lls. 4-11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to stack at least two of the IC packages disclosed by Rokugawa (i.e. having a second substrate positioned in stacked fashion on the first coverlay; a second IC mounted on a surface of the second substrate; a second coverlay laminated on the surface of the second substrate and having at least one opening formed by photolithography wherein the second IC is positioned in the opening formed by photolithography) and to connect the ICs in accordance with Fox's invention in order to increase the package mounting density and to connect a communication device such wireless data transceiver to the first and/or second IC disclosed by Rokugawa in view of Fox to permit remote interrogation of the chip as taught by Blumenau. Note that the first and second substrates are equivalent.

18. Regarding claim 21, Rokugawa in view of Fox further in view of Blumenau teaches that the first and second coverlays are made of a flexible material. Note that Rokugawa shows that the coverlay is a flexible material such polyimide and copper (col. 7/lls. 9-24 & col. 14/lls. 47-54)

19. Regarding claims 22 and 39, Rokugawa in view of Fox further in view of Blumenau teaches that the first and second substrates are made of a flexible material.

Note that Rokugawa shows that the substrate is a flexible material such polyimide and copper (col. 7/lls. 9-24 & col. 14/lls. 47-54).

***Response to Arguments***

20. Applicant's arguments filed 8/12/2005 have been fully considered but they are not persuasive. Applicant argues that the insulation layer disclosed by Rokugawa is not formed by a lamination process. Nevertheless, this limitation is not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The term "coverlay laminated" has been interpreted as a structural description and not as a process limitation. As shown by Rokugawa (e.g. fig. 17) the substrate 14 and the coverlay 14 is a laminated structure since they are composed of laminae. In any case, a "product by process" claim is directed to the product per se, no matter how actually made. See *In re Thorpe et al.*, 227 USPQ 964 (CAFC, 1985) and the related case law cited therein which makes it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe, even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington*, 411 F.2d 1345, 1348, 162 USPQ 145, 147



(CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935).

21. Applicant argues that the superposed insulating layers 14 are not in contact with each other. Nevertheless, *Rokugawa* clearly teaches that the insulating layers 14 are in contact with each other (e.g. fig. 6A & 17).

22. Applicant argument that *Rokugawa* does not show an IC being in a hole. Nevertheless, the flexible layer 41 can be considered part of the coverlay. Therefore, the IC is located in an opening formed by photolithography (e.g. fig. 16 and col. 14/lis. 1-15).

### ***Conclusion***

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-

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1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

25. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

26. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Leonardo Andujar  
Primary Examiner  
Art Unit 2826